ABSTRACT OF THE DISCLOSURE

The invention provides a semiconductor memory device comprising a plurality of word lines, a plurality of bit lines, and a plurality of static memory cells each having a first, second, third, fourth, fifth, and sixth transistors. While each of channels of the first, second, third, and fourth transistors are formed vertical against a substrate of the semiconductor memory device. Each of semiconductor regions forming a source or a drain of the fifth and sixth transistors forms a PN junction against the substrate. According to another aspect of the invention, the SRAM device of the invention has a plurality of SRAM cells, at least one of which is a vertical SRAM cell comprising at least four vertical transistors onto a substrate, and each vertical transistor includes a source, a drain, and a channel therebetween aligning in one aligning line which penetrates into the substrate surface at an angle greater than zero degree.